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# A SWITCHED-CAPACITOR FRONT-END FOR VELOCITY-SELECTIVE ENG RECORDING

R. Rieger, *Senior Member, IEEE*, and J. Taylor, *Member, IEEE*

**Abstract**— Multi-electrode cuffs (MECs) have been proposed as a means for extracting additional information about the velocity and direction of nerve signals from multi-electrode recordings. This paper discusses certain aspects of the implementation of a system for *velocity selective recording (VSR)* where multiple neural signals are matched and summed to identify excited axon populations in terms of velocity. The approach outlined in the paper involves the replacement of the digital signal processing stages of a standard delay-matched VSR system with analogue switched-capacitor (SC) delay lines which promises significant savings in both size and power consumption. The system specifications are derived and two circuits, each composed of low-noise preamplifiers connecting to a 2<sup>nd</sup> rank SC gain stage, are evaluated. One of the systems provides a single-ended SC stage whereas the other system is fully differential. Both approaches are shown to provide the low-noise, low-power operation, practically identical channel gains and sample delay range required for VSR. Measured results obtained from chips fabricated in 0.8  $\mu\text{m}$  CMOS technology are reported.

**Index Terms**— Biomedical electronics, Neural prosthesis, Implantable biomedical devices, Nerve Signal (ENG) Recording, Velocity Selective Recording (VSR), CMOS integrated circuit

## I. INTRODUCTION

VELOCITY selective recording (VSR) has been suggested as a method to increase the functionality of neural (ENG) recording and, therefore, potentially to increase the scope for employing naturally occurring (afferent) neural signals to provide sensory feedback to artificial devices [1], [2]. This subject is currently a major challenge in neuroprosthetics research [3] - [6]. The origin of the problem lies in the fact that a single *tripolar* nerve cuff (nerve cuff electrodes are currently the most well-established long-term interfaces) provides only one output signal and hence the information that can be acquired is limited. Given the large number of fibres in each peripheral nerve, this reduction represents a huge loss of information. One possible method for addressing this problem uses *fibre diameter-selective recording*, which is equivalent to measuring the level of activity in the *velocity* domain, i.e.

VSR. This requires more information and in order to overcome the data acquisition limitation of single tripoles, the use of *multi-electrode cuffs* (MECs) has been proposed [1]. An MEC is an extension of a single tripolar nerve cuff to one containing several ( $N$ ) dipoles from which  $N-1$  tripolar signals can be obtained. Conventionally, tripolar signals are obtained using a double-differential amplifier arrangement [7]. Action Potentials (AP) propagating with different velocities  $v$  along the nerve appear in the tripolar output signal with characteristic delays  $T = d/v$ , where  $d$  is the electrode pitch. If equal and opposite delays are introduced subsequently by the signal processing, and the tripole signals are added, the resulting output *power* is a maximum for that conduction velocity [1]. This allows the system *in principle* to classify excited populations by their propagation velocities. A system using an MEC to achieve VSR has been described recently and demonstrated *in vitro* in frog nerve [8].

In this system, the outputs of the second rank amplifiers are digitised and transmitted to a second, entirely digital ASIC by implanted cables which also allow commands and power to be fed back to the first ASIC. The second ASIC is a digital demultiplexing system which also converts the bipolar (single differential) data from the first ASIC, converts to *tripolar* (double differential) form and implements the signal processing operations (delay, add, bandpass filtering) required

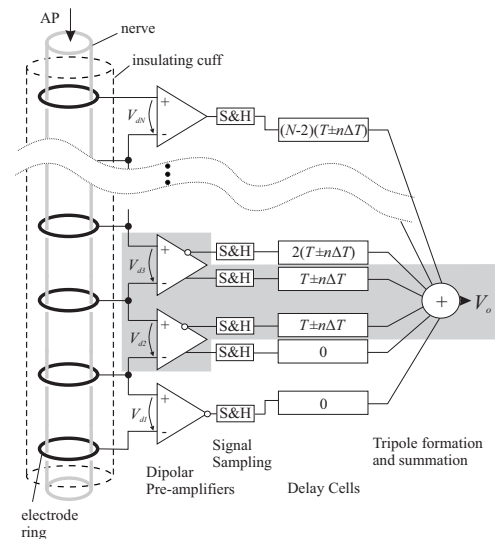


Fig. 1: Multi-electrode cuff (MEC) connected to the proposed multi-channel amplifier array and delay stages to implement velocity selective recording (VSR). The two outermost channel gains must be matched. The delay stages provide nominal inter-channel delay  $T$  which is variable in  $n$  steps  $\Delta T$ .

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R. Rieger is with the Electrical Engineering Department of National Sun Yat-Sen University, 70 Lien-Hai Road, 804 Kaohsiung, Taiwan (e-mail: rieger@mail.nsysu.edu.tw).

J. Taylor is with the Electronic and Electrical Engineering Department of University of Bath, BA2 7AY Bath, UK (e-mail: j.t.taylor@bath.ac.uk).

in VSR to compute the *velocity spectrum*. These processes are quite costly in terms of power consumption and die area. For example in a typical 10-channel VSR system realised in 0.35  $\mu\text{m}$  CMOS technology, the ‘basic’ functions (MUX/DMUX etc) consume about 40 mW, adding the signal processing functions required for VSR adds a further 70 mW and more than doubles the die area [9][10].

In this paper we propose the use of analogue delay lines to carry out the VSR signal processing and we derive the target specifications for this system. A single-ended switched-capacitor (SC) circuit previously described in [11] is evaluated to establish its practicality for VSR. In addition, a fully differential version of this circuit is presented and its performance compared with that of the earlier circuit. A very significant saving in power consumption results compared to the fully digital system. This is very advantageous for an implanted device.

## II. SYSTEM SPECIFICATION AND DESIGN

For a delay-matched VSR front end, each tripolar channel signal of a particular velocity  $v$  is delayed by a time interval  $T$  with respect to the next channel. Instead of introducing the delay after the formation of tripoles as in the conventional structure [1] we propose to delay the constituent dipole signals before summation as shown in Fig. 1. This allows us to employ the programmable delay-and-add structure presented in this paper realized as a SC sample-and-hold circuit (S&H). Summation of the appropriately delayed dipoles yields the summed tripolar output required for VSR [2]. For a system with  $N+1$  electrodes, there will be  $N$  dipolar signals and  $N-1$  tripolar ones. The total delay at velocity  $v$  will therefore be  $(N-2)T$ , normally realized digitally. In order to achieve delay matching, the first channel (i.e. the channel where the AP arrives first) will have the maximum delay and the  $(N-1)$ th, zero delay. The required delay for each dipole channel is determined by the velocity range to be discriminated and the geometry of the cuff. For example, for a velocity range  $30 \leq v \leq 100$  m/s, with a cuff length 1.8 cm and  $N=10$ , the inter-tripolar spacing,  $d$ , is 2 mm and the required range of inter-tripolar delay is  $20 \mu\text{s} \leq T \leq 66.7 \mu\text{s}$ . For delay matching, the maximum delay that must be realized will be determined by the lowest velocity to be discriminated (30 m/s in this case) and is  $T_{MEC} = 600 \mu\text{s}$  for this system (the other  $N-2$  lines will

have delay lengths 0.533, 0.467, ... 0.067, 0 ms).

The step on the velocity axis sets the precision at which the velocity spectrum can be calculated. If it was desired not only to detect activity at one given velocity but also to determine a wider velocity spectrum, the delays should be made variable. The delay variation in each line is determined by the chosen velocity resolution and can be expressed as  $\tau = n\Delta T$ , where  $\Delta T$  is the delay step and  $n$  is an integer. To explain this, consider two adjacent points on the velocity axis:  $v$  and  $v - \Delta v$  where  $v$  is a matched velocity and  $\Delta v$  is the velocity step. The delay step  $\Delta T$  corresponding to the velocity offset  $\Delta v$  is given by (1):

$$\frac{\Delta T}{T} = \frac{\Delta v}{v - \Delta v} \quad (1)$$

Rearranging (1) yields:

$$\frac{\Delta v}{v} = \left( \frac{\Delta T / T}{1 + \Delta T / T} \right) \quad (2)$$

and we define the factor  $\Delta v/v$  as  $R_v$ , the *velocity resolution*. It represents the minimum step on the velocity scale and is important as an indicator of the usefulness of the VSR method. As a practical example choose  $R_v$  to be  $\leq 0.1$  for all matched velocities in the range quoted above. Then from (2),  $R_v$  will increase with decreasing  $T$ , i.e. as matched velocity  $v$  increases (the difficulty of preserving velocity resolution at high velocities has often been noted). So, e.g., for a matched velocity of 100 m/s ( $T = d/v = 20 \mu\text{s}$ ) and if  $R_v = 0.1$ , from (2)  $\Delta T = 2.2 \mu\text{s}$ . At the other end of the scale,  $\Delta T = 7.4 \mu\text{s}$  is required for the lowest velocity of 30 m/s.

Practically, the maximum delay that can be implemented using a simple S&H is limited by the sampling interval. The sampling interval  $T_s$  is ultimately determined by the bandwidth of the analogue input signal and given that the bandwidth of interest is from about 100 Hz to at least 5 kHz, the sampling rate should be above 10 kHz, limiting the maximum achievable delay  $T_{MEC}$  to less than 100  $\mu\text{s}$ . For the 2 mm electrode pitch used in our example this delay would limit the channel count to  $N=2$ , i.e. a single matched tripole output. To extend the system to multiple tripoles, additional processing channels (excluding the power hungry low-noise pre-amplifiers) may be placed in parallel. Offsetting the sampling time of each parallel system by  $T_s$  increases the effective sample rate as the output is multiplexed between the parallel channels. Analysis of the system in Fig. 1 shows that the summed tripole system output voltage is given by

$$\begin{aligned} V_o &= \sum_{i=1}^{N-1} (V_{d,i+1} - V_{d,i})^{i-1} \\ &= -(V_{d1}^0 + V_{d2}^1) + (V_{d2}^0 + V_{d3}^1) - (V_{d3}^2 + V_{d4}^3) + \dots \end{aligned} \quad (3)$$

where the superscript denotes the unit time delay ( $\tau$ ) of the dipole. The expression represents a sum of pairs of adjacent dipoles with a unit delay between paired channels. In this paper we discuss the implementation of one pair of recording channels as indicated by the shaded area in Fig. 1. We seek to establish that an SC circuit from [11] and its fully differential extension can be used to implement the delayed and summed dipole pair which is fundamental to implementing VSR.

The outline schematic of the differential recording channel

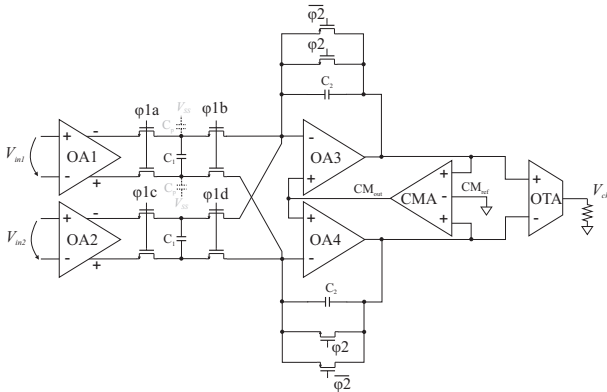


Fig. 2: Circuit schematic of the system using a differential SC stage.

pair is shown in Fig. 2. The circuit consists of two continuous-time preamplifier stages OA1 and OA2 providing a voltage gain of about 70 V/V. These continuous-time buffers are designed for low-noise operation and have been discussed in [8]. *Lateral* bipolar transistors (BJTs) are used in the input stage. These devices possess many of the advantageous properties of standard (vertical) BJTs. In particular, they provide an optimal trade-off between low noise and low power consumption that is crucial in this application. Also shown in the schematic are the parasitic capacitances  $C_p$  associated with the sampling capacitors of channel 1. Parasitic capacitances are also present in the other channel but are not shown in the figure for clarity. Using the tripole recording setup the difference between adjacent channel outputs is obtained and common-mode (CM) interference is rejected if all channels yield identical gain. Since it is the gain matching between the outermost channels that mostly determines the overall rejection of CM signals, it is important to equalize the gains of those channels to about  $\pm 1\%$ . The low-noise pre-amplifiers provide these well-matched channels as described in [11]. The preamplifiers connect to a 2<sup>nd</sup> rank SC gain stage to implement the delay and summation and to provide additional gain. The overall voltage gain of the recording channel is chosen to be around 60 dB. As the amplitude of the recorded nerve signal is affected by many factors (including cuff geometry and interface impedance) the absolute gain is not critical.

TABLE I: SPECIFIED AND MEASURED SYSTEM PERFORMANCE DATA FOR  $N=2$ . ESTIMATE VALUES FOR DIGITAL AND ANALOGUE FRONT-ENDS ARE SHOWN FOR COMPARISON (SYSTEMS REPORTED IN [9], [11]).  $0.8 \mu\text{m}$  CMOS TECHNOLOGY AND  $\pm 2.5 \text{ V}$  SUPPLY IS ASSUMED FOR ALL DESIGNS.

	Specified	Measured single-ended	Measured differential	Amplifier + Digital processor	Analogue front-end (no VSR)
Differential gain	600 – 1000	607	$360/A_{\text{buffer}} \approx 900^{\#}$	10,100	10,100
Gain mismatch	$< \pm 1\%$	$< \pm 0.75\%$	$< \pm 0.75\%$	$\pm 0.75\%$	-
CMRR	$> 80 \text{ dB}$	100 dB	$> 151 \text{ dB}$	100 dB	82 dB
CM input range	$> \pm 250 \text{ mV}$	$> \pm 400 \text{ mV}$	$> \pm 400 \text{ mV}$	-	-
Channel crosstalk	$< 5\%$	$< 0.1\%$ , (7% with incomplete reset)	$< 0.1\%$	-	$< 0.9\%$
Sample rate, effective BW	$\geq 10 \text{ kHz}$ , 5 kHz	10 kHz, 5 kHz	10 kHz, 5 kHz	34 kHz, 17 kHz	-, 3.3 kHz
Input noise	$\ll 100 \text{ nV}/\sqrt{\text{Hz}}$	14.3 nV/ $\sqrt{\text{Hz}}$	14.3 nV/ $\sqrt{\text{Hz}}$	4.1 nV/ $\sqrt{\text{Hz}}$	3.8 nV/ $\sqrt{\text{Hz}}$
SNR [dB]	$\gg 20$	$\sim 60$	$\sim 60$	71	90
Power per channel	$< 2 \text{ mW}$	1.4 mW	1.7 mW	15 mW	2.4 mW
Overall channel area	-	0.42 mm <sup>2</sup>	0.43 mm <sup>2</sup>	2.7 mm <sup>2</sup>	1.2 mm <sup>2</sup>
Delay&Add Area/Channel	-	0.05 mm <sup>2</sup>	0.06 mm <sup>2</sup>	1.6 mm <sup>2</sup>	
Detection velocity [m/s]	30 - 100	39 - 300	39 - 300	1 - 30	
Velocity Resolution	$\leq 0.1$	0.06 - 0.2	0.06 - 0.2	0.03-0.5	
Delay $T$ [ $\mu\text{s}$ ]	20 - 67	5 - 80	5 - 80	100-3000	
$\Delta T$ [ $\mu\text{s}$ ]	2.2 - 7.4	5 - 80 <sup>*)</sup>	5 - 80 <sup>*)</sup>	100	
$\sigma_t$ [ $\mu\text{s}$ ]	$\ll 3$	$< 1^*)$	$< 1^*)$	-	

<sup>\*)</sup> Microcontroller generated

<sup>#)</sup> Approximate result as  $A_{\text{buffer}}$  is not precisely established in this setup.

The remaining system parameters are chosen to yield a performance comparable to previously reported systems [8][9][11]. The specification is summarized in Table I. Note that although several amplifier arrays for physiological signal recording have been reported in the literature ([12]-[19]), these arrays are often specifically targeted at the recording of intracortical activity and do not match inter-channel gain or provide a specified sampling delay.

#### A. Front-end systems

In the system of Fig. 2 the preamplifiers differentially charge the sampling capacitors  $C_1$  when the sampling switches are closed during phases  $\phi 1a$  or  $\phi 1c$  for channel 1 and channel 2 respectively. Since the timing of the front-end sampling phases is programmable, it is possible to combine the implementation of the delay function with the sampled-data analogue front-end. In the amplification phase either switches  $\phi 1b$  or  $\phi 1d$  are closed, routing the respective recording channel to the system output. The switches across  $C_2$  are open during this phase and the circuit is configured as a charge amplifier providing a nominal voltage gain of  $C_1/C_2$  whose accuracy is determined by on-chip capacitor matching. After the charge transfer has completed and voltage  $V_{ch}$  is obtained the feedback capacitor is cleared by closing the transmission gate in phase  $\phi 2/\overline{\phi 2}$ . The phasing of the switches used in this implementation is shown in Fig. 3. The period of the clock is  $100 \mu\text{s}$ , corresponding to a sample rate of 10 kHz per channel. The circuit is symmetrical during both phases. Therefore, capacitors  $C_1$  are also laid out symmetrically and equal parasitic capacitance  $C_p$  results at all circuit nodes. Since the symmetry of the circuit is maintained also in the amplification phase, the input voltages at the negative terminals of OA3 and

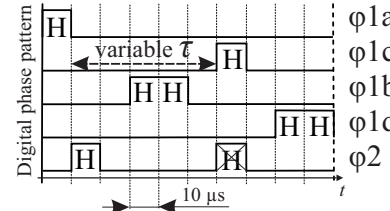


Fig. 3: Phase pattern of the digital switch control signals with variable delay  $\tau$ . The sequence repeats after  $100 \mu\text{s}$ . Removing the second pulse of  $\phi 2$  realizes channel summation. Inverted phases are also generated as required.

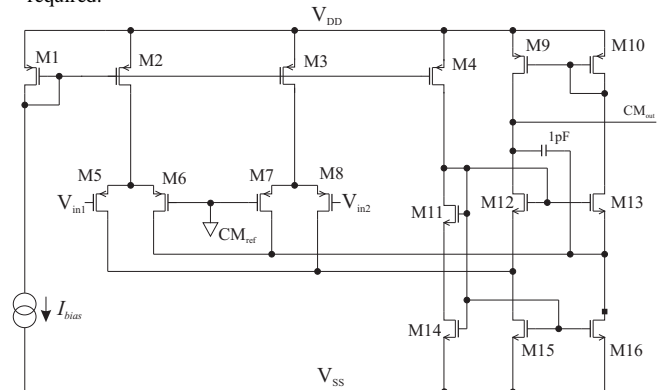


Fig. 4: Circuit schematic diagram of the common-mode amplifier used in the fully differential SC stage.



OA4 at the beginning of the charge transfer phase are  $V_{out1}$  and  $V_{out2}$  respectively. The overall circuit gain is given by:

$$V_{ch} = 2 \frac{C_1}{C_2} (V_{out1} - V_{out2}) \cdot A_{buffer} \quad (4)$$

where  $A_{buffer}$  is the gain of an output buffer described later. This result applies irrespective of the absolute magnitude of the parasitic capacitance in the sampling stage.

The CM level at the positive terminals of OA3 and OA4 is stabilized using the CM amplifier CMA to analogue ground ( $V_{gnd\_a}$ ), which is half-way between the  $\pm 2.5$  V supplies  $V_{DD}$  and  $V_{SS}$ . OA3 and OA4 are conventional folded-cascode amplifiers [11]. The circuit schematic diagram of the CM amplifier is shown in Fig. 4. It is a folded-cascode structure with a duplicated input stage consisting of transistors M5-M8 to generate the CM error signal. Devices M11-M16 form a *pseudo cascode* [20] by making the cascode transistor aspect ratio large compared to the mirror transistors M14-M16. The chosen dimensions are  $6\mu\text{m}/2\mu\text{m}$  and  $30\mu\text{m}/1\mu\text{m}$  for mirror and cascode transistors respectively. The bias current  $I_{bias}$  is  $1\mu\text{A}$ . A  $1\text{pF}$  feedback compensation capacitor is added to ensure an adequate phase margin.

In order to ease measured evaluation of this circuit an output buffer is added which performs differential to single-ended conversion. As absolute gain is not critical an open-loop transconductance stage is chosen which terminates in an off-chip  $6.2\text{ k}\Omega$  load resistor for a nominal gain  $A_{buffer}$  of  $1/2$ . Using a forward structure makes both input terminals available for differential to single-ended conversion but trades this off with potentially high distortion limiting the available output range to approximately  $100\text{ mV}_{pp}$ , which is deemed acceptable for this test implementation. Note, this output stage would not be required in a final application connecting directly to an ADC.

As an alternative configuration to the system using a fully differential SC stage a second, single-ended arrangement is considered with a circuit as shown in Fig. 5. This system was described in [11].

The parasitic capacitances  $C_{pa}$  and  $C_{pb}$  at these sampling nodes are dominated by a bottom plate parasitic capacitance of  $C_l$  and can be denoted by fractions  $\alpha$  of the nominal capacitance  $C_l$ , so that  $C_{pa} = \alpha_a C_l$  and  $C_{pb} = \alpha_b C_l$ . Circuit analysis shows that the channel output voltage yields:

$$V_{ch} = \frac{C_1}{C_2} ((\alpha_b + 1)V_{out1} - V_{out2}) \quad (4)$$

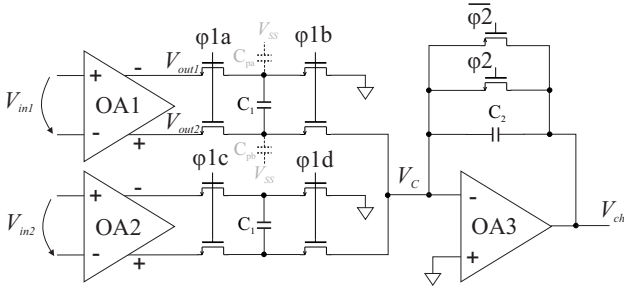


Fig. 5. The circuit schematic used for simulation. It consists of two first-rank amplifiers OA1 and OA2 and one switched capacitor multiplexer unit showing the connection to the second rank amplifier, OA3.  $C_1$  is  $10\text{ pF}$  and  $C_2$  is  $1\text{ pF}$ , providing a voltage gain of 10.

This result reveals that the CM rejection of the SC stage (i.e. when  $V_{out1} = V_{out2}$ ) is affected by the parasitic capacitance. It is therefore important that the CM feedback circuit of the input stage tightly controls the CM voltage to be equal to the reference ground voltage used in the SC stage.

### B. Noise performance

Very-low noise performance of the circuit is crucial for the recording of the ENG where input signal amplitudes are in the micro-volt range. The signal-to-noise ratio (SNR) target is required to be considerably higher than about 10 to yield useful results for VSR. This also sets a limit to the voltage noise spectral density of the recording system to much less than  $100\text{ nV}/\sqrt{\text{Hz}}$ . The preamplifiers establish a continuous-time noise floor lower than  $15\text{ nV}/\sqrt{\text{Hz}}$  [8]. Since the SC stage follows after the signal has been preamplified,  $kT/C$ -noise of the switches remains negligible. However, sampling noise due to aperture jitter caused by timing variation of the falling edges of phases  $\phi 1a$  and  $\phi 1b$  must be taken into account. Assuming a sinewave input, the worst-case SNR degradation due to clock jitter can be estimated. It has been shown that this SNR is given by  $(\sigma_i 2\pi f)^{-1}$  [21], where  $\sigma_i$  denotes the standard deviation of clock jitter and  $f$  the input signal frequency. Thus, for our system  $\sigma_i$  is required to remain below  $3\mu\text{s}$ .

## III. SIMULATED RESULTS

The arrangements used for simulation are the circuits shown in Figs 2 and 5 consisting of a pair of dipole channels multiplexed to a 2<sup>nd</sup> rank SC stage. This was simulated using  $0.8\mu\text{m}$  CMOS transistor models and the Cadence Spectre circuit simulator. Parameter estimates for the lateral input device are used, and the simulated results for the input stage are comparable to the data reported in [8]. The total input-referred spot noise density at  $1\text{ kHz}$  is estimated as  $8.4\text{ nV}/\sqrt{\text{Hz}}$ .

For the single-ended SC stage simulation with  $C_l = 10\text{ pF}$  and  $C_2 = 1\text{ pF}$  yields a differential voltage gain of  $9.6\text{ V/V}$ . The CM to differential gain simulated by introducing top and bottom plate parasitic capacitances into the circuit schematic using  $\alpha_a = 10\%$  and  $\alpha_b = 5\%$  yields  $-9.2\text{ dB}$ .

The fully differential SC stage was simulated with parasitic capacitances  $\alpha_a = \alpha_b = 10\%$  and, as before,  $C_l$  was chosen to be  $10\text{ pF}$  and  $C_2$   $1\text{ pF}$ , providing a nominal gain of  $20\text{ V/V}$ . The simulated output stage gain is  $0.49$  with a cut-off frequency of  $642\text{ kHz}$  when loaded with  $40\text{ pF}$ . The gain variance of the output stage is found by Monte-Carlo simulation to be  $3\%$  and the SC stage gain variation depends on capacitor matching.

The simulated gain of each complete single-ended channel was  $810\text{ V/V}$ , depending strongly on the estimate made for the input BJT transconductance. The channel crosstalk is  $-110\text{ dB}$  and the power consumption per channel  $2\text{ mW}$  which is somewhat less than that reported in [8]. Note however, that this advantage will increase with the number of channels in the system.

For the differential channel the simulated overall gain is  $775\text{ V/V}$  in agreement with (4). The additional circuit blocks OA4, CMA and output stage OTA increase the power consumption

of the differential system by 320  $\mu\text{W}$  (160  $\mu\text{W}$  per channel) compared to the single-ended SC stage.

#### IV. MEASURED RESULTS

The systems were implemented on a test chip using austriamicrosystems 0.8 $\mu\text{m}$  double-metal single-poly (2M1P) CMOS technology. As in the arrangement used for simulation, the test chip contained two preamplifiers (1<sup>st</sup> rank), one single-ended SC stage and one differential SC stage with output stage. The front-end amplifiers occupy an active area of approximately 0.74  $\text{mm}^2$ , the single-ended SC stage 0.13  $\text{mm}^2$  and the differential SC stage 0.28  $\text{mm}^2$  (0.19  $\text{mm}^2$  excluding the output buffer). Fig. 6 is a photomicrograph of the chip. The preamplifier gains were measured on 3 different dies confirming that the channels are closely matched as expected with a relative gain mismatch of less than  $\pm 0.75\%$ . A frequency sweep allowed the -3 dB cut-off frequency of the preamplifiers to be determined at around 15 kHz. The measurements on the complete channel using the single-ended SC stage and which are reported below confirm this performance of the input stage. The second step was to evaluate the single-ended SC stage by applying the test signals directly to the sampling switches after the amplifiers OA1/OA2. As there is no hold-stage implemented on the test chip, the SC output voltage was sampled just before the positive edge of phase  $\phi_2$  using a data acquisition system (LabView with NI 6250 DAQ card). This captures the voltage at a sample time just before the capacitors are reset, which is representative of the final application which employs sampling by the analogue-to-digital converter (ADC). A microcontroller (PIC) was programmed to generate the clock phases shown in Fig. 3 and connected to the ASIC under test. A 200 mV<sub>pp</sub>, 100Hz sinewave was applied differentially to the SC stage resulting in a sampled output signal amplitude of 832 mV<sub>pp</sub>, yielding a gain of 4.2. This is considerably smaller than the expected gain of 10. On closer inspection it was found that the additional capacitive load of the test board and probes increased the settling time of the SC amplifier from the designed value of 10  $\mu\text{s}$ , so that the output signal is sampled before complete settling is achieved. After the clock speed was slowed down to allow for 30  $\mu\text{s}$  settling, the measured gain increased to 9, close to the targeted value. It is anticipated that in the final application where the amplifier output drives only the small load of an on-chip ADC the correct gain is obtained at full sample speed. The CM gain of the stage is measured as -9.1 dB resulting in a CM rejection of at least 23 dB.

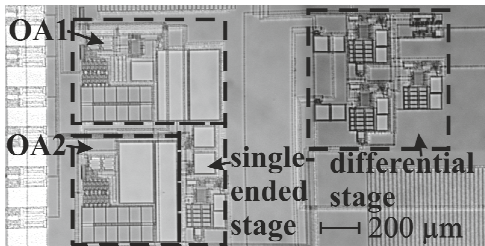


Fig. 6: Microphotograph of the test chip realized in 0.8  $\mu\text{m}$  CMOS technology.

The next step was to evaluate the complete system including both pre-amplifiers and the SC-stage. To obtain the full channel gain the clock pattern was rearranged. Additional 10  $\mu\text{s}$  idle periods were inserted after the negative edge of  $\phi_{1b}$  and  $\phi_{1d}$  respectively yielding a longer output settling time before the stage is cleared. This stretches the phase pattern to 120  $\mu\text{s}$  yielding a sample rate of 8.3 kHz. Fig. 7.a shows the recorded output voltage spectral density for the two channels when a 200 Hz sinusoid is applied to channel 1 and a 2 kHz signal to channel 2. Both sinusoidal input amplitudes are 2.8 mV<sub>pp</sub> and the output amplitudes are 1.7 V<sub>pp</sub>, confirming a channel gain around 607. Fig. 7.b shows the transient measured results for this setup. The figure shows that the two channels can be resolved and separated successfully after passing through the shared stage.

The crosstalk between the channels was initially measured to be just below 7%. This relatively large value is attributed to the higher than expected load capacitance of the measurement setup. From simulation a 180 pF load results in 7% crosstalk for typical transistor parameters. Again, this would be less of a problem in an application where the node  $V_{ch}$  is not pinned out. Indeed, increasing the reset phase  $\phi_2$  from 10  $\mu\text{s}$  to 30  $\mu\text{s}$  reduced the measured crosstalk to below 0.1%.

The total harmonic distortion (THD) was measured for a large output amplitude of 4.3 V<sub>pp</sub> to be around -90 dB. The channel noise was evaluated by connecting both the pre-amplifier inputs to the reference ground potential and observing the output voltage using a spectrum analyzer. Referring back to the system input by dividing through the

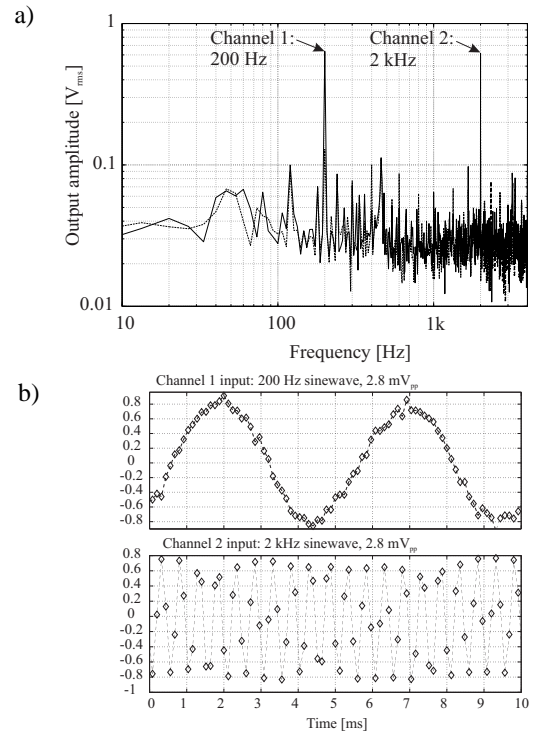


Fig. 7: a) FFT plot of single-ended system measured output data sampled 38  $\mu\text{s}$  after the positive edges of phase  $\phi_{1b}$  and  $\phi_{1d}$  respectively, splitting the output into two channels. A 200 Hz sinewave was applied on channel 1 (top) and a 2 kHz sinewave on channel 2 (bottom). Both input amplitudes are 2.8 mV<sub>pp</sub>. b) Corresponding transient plot of the measured data.

channel gain yields around  $1.0 \mu V_{rms}$  total noise in a bandwidth 100 Hz-5 kHz, which is equivalent to  $14.3 \text{ nV}/\sqrt{\text{Hz}}$  average input spot noise density.

In a further step the differential SC stage with output buffer is evaluated, at first separately from the preamplifiers. The original clock pattern of Fig. 3 is applied in these measurements. Applying 25 mVpp, 100 Hz sinusoids through a resistive divider with a gain  $1/11.4$  to yield 8.77 mVpp differentially at the SC stage input results in a measured output amplitude of 61 mVpp. The resulting differential gain is thus 7 V/V. This is in agreement with an expected SC stage gain of 20 V/V followed by a nominal output stage gain of  $1/2$  which, however, due to the open-loop approach is not tightly controlled. The CM to differential gain was observed to be -40 dB giving a CM rejection of 56 dB. As expected this figure is considerably higher than that measured for the single-ended stage.

Finally, the complete differential channel including front-end amplifiers was evaluated. The differential gain including buffer is 360 V/V and the CM rejection exceeds the measurement range of the test equipment with over 151 dB. The differential gain remains constant over the entire recording bandwidth which was confirmed with a frequency sweep. The channel crosstalk is measured with a 100 Hz, 850  $\mu V_{pp}$  sinusoidal input and yields less than 0.1%. The harmonic distortion was measured for a sinusoid at 100 Hz. Owing to the small output range of the buffer stage a 40 mVpp output amplitude is chosen. The measured THD is approximately 2.5%. However, at this small signal level this is on the order of the harmonic distortion produced by the test signal generator at the system input. Therefore, the measured THD can be considered an upper bound.

The measured performance data of the system are summarized in Table I in comparison with the specification. Additional measured results for the individual stages are given

TABLE II: MEASURED AND SIMULATED RESULTS FOR THE INDIVIDUAL STAGES. OVERALL MEASURED RESULTS ARE SHOWN IN TABLE I.

Input stage, all measured results			
Differential Gain	67 V/V	Differential i/p range	12 mV <sub>pp</sub>
CM gain	-64.7 dB	Input noise	14 nV/ $\sqrt{\text{Hz}}$
CMRR	101 dB	-3dB frequency	~15 kHz
Channel gain mismatch	< $\pm 0.75\%$	Channel crosstalk	< 0.1%

Single-ended SC-stage	Measured	Simulated
CM input range	> $\pm 400 \text{ mV}$	-
Differential gain	9	9.6
CM gain	-9.1 dB	-9.2 dB ( $\alpha_b=5\%$ )
CMRR	28 dB	28.8 dB
THD	-90 dB (4.3 Vpp output)	-
Area	0.13 mm <sup>2</sup>	0.13 mm <sup>2</sup>

Differential SC-stage inclusive output stage with gain $1/2$		
	Measured	Simulated
CM input range	> $\pm 400 \text{ mV}$	-
Differential gain	9.7 V/V	10 V/V
CM gain	-40 dB	-41 dB
CMRR	60 dB	61 dB
THD	< -32 dB (40 mV <sub>pp</sub> output)	-
Area	0.28 mm <sup>2</sup>	0.28 mm <sup>2</sup>

in Table II. A comparison between the single-ended and fully differential system show that, although high CM rejection is obtained for the differential system, also the performance of the single-ended approach is suitable for the target application.

The delay property of the circuit was confirmed by introducing different delays between phases  $\phi 1a$  and  $\phi 1c$ . Lissajous plots, where the normalized measured output voltage of channel 1 is plotted on the horizontal axis versus the output voltage of channel 2 on the vertical axis, are given in Fig. 8 for the double-differential system. Equivalent plots could be obtained for the single-ended stage. The increased inter-channel delay shows in these plots as decreasing eccentricity of the ellipse, confirming programmable delay between 5 and 80  $\mu\text{s}$ .

As a further practical demonstration, single traveling APs are synthesized using a template [22] and applied to the SC stage using the test setup shown in Fig. 9. An example of the resulting dipole voltages obtained at adjacent electrodes (2 mm equivalent pitch) for two velocities is shown in Fig. 10. The clock pattern is programmed to delay the second dipole output compared to the first dipole and to sum the dipole outputs to obtain a dipole pair described by (3). Summation is realized by removing the second phase  $\phi 2$  pulse (Fig. 3) so the integrating capacitor is cleared only after both dipoles have been sampled and transferred to the output stage.

Firstly, the clock phases match the system to a velocity of 25 m/s. In a second measurement, the system is matched to 50 m/s. In both setups, the measured peak-to-peak output voltage is measured and plotted. This is repeated for different velocities of the synthesized AP yielding the spectra shown in Fig. 11. The 25 m/s matched system yields a clear peak at the matched velocity. The 50 m/s matched system yields a broad maximum at higher velocities. This agrees with the velocity spectrum obtained analytically and which is also shown in Fig. 11 evaluated at a spectral frequency of 5 kHz. Clearly, the velocity selectivity of a dipole pair is quite low. However, they constitute the basis for implementing VSR by adding several such dipoles to yield the desired transfer function [1].

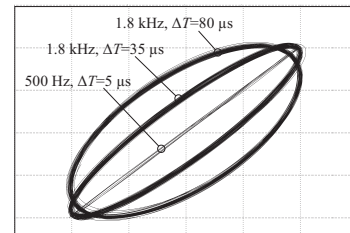


Fig. 8: Lissajous plots of the SC-stage channel output voltages for identical sinewave inputs. Variation of sampling phase delays yields the interchannel delays  $\Delta T$ .

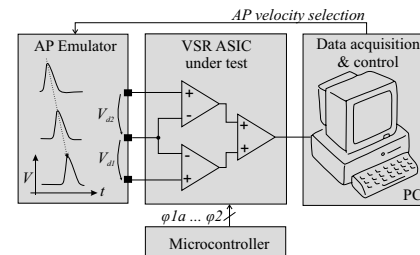


Fig. 9: Diagram of the setup for bench testing the ASIC with synthesized AP.

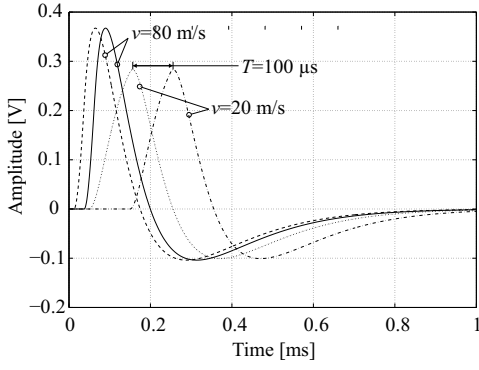


Fig. 10: Example of synthesized traveling dipole AP voltages ( $V_{d1}$ ,  $V_{d2}$ ) with 20 m/s and 80 m/s velocity obtained at adjacent electrodes (2 mm equivalent pitch). The synthesized signal is used for testing the SC stage transfer function.

## V. DISCUSSION AND CONCLUSIONS

In this paper a method to improve the design of implantable VSR systems has been proposed. A new metric for VSR theory is proposed which we call *velocity resolution*, i.e. the minimum velocity step available for spectral analysis. Based on this metric a specification for the recording channel with VSR capability is derived. Also, it was previously shown that MEC-based systems have potentially much better interference (i.e. EMG and other *common-mode* signals) suppression characteristics than single *tripoles* and that in fact the only significant contributions originate from the two end electrodes of the array. It follows from this that interference suppression is optimised if the gains of the outermost channels of the array are equalised.

SC gain circuits with matched gain for the recording of very small signals with the target application of capturing the ENG from a MEC are discussed. Sampled-data analogue techniques not only eliminate most of the gain error between channels but also allow the phase difference to be selected by setting individual sample points for each channel for tuning in to a selected frequency recording range [1]. In the single-ended version the pre-amplified differential signal is converted to a single-ended voltage by reconnecting one side of the sampling capacitor to a reference ground level during the charge transfer phase. However, this degrades the CM rejection and can lead to high offset voltages at the channel output if the CM level of the preamplifiers is not well matched to the reference ground level used in the SC stage. In the circuits evaluated here, the resulting offset voltage was small. However, in a future design with more channels added, sharing a single CM amplifier whilst maintaining this good result may become more challenging. The presented fully differential circuit alleviates this potential problem at the cost of requiring an additional CM circuit in the SC stage.

Several critical issues in the circuit design for VSR have been identified in this study. Firstly, the circuit design was targeted at the final application where the channel outputs interface with an on-chip ADC and measurement revealed that the single-ended system was slightly under-designed to drive the larger capacitive load of the test equipment. This led to

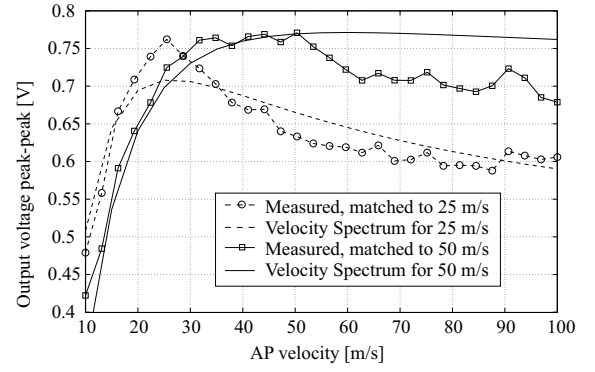


Fig. 11: Measured system output amplitude for two matched velocities versus AP velocity. The velocity spectra of the dipole pair obtained analytically (amplitude evaluated at 5 kHz, arbitrary units) are shown for comparison.

incomplete settling of the output voltage and incomplete reset of the gain capacitor. As a result, the channel gain was reduced from the target value and channel crosstalk was increased.

Secondly, to achieve sufficient sampling rate for multiple tripole outputs ( $N > 2$ ) several SC stages would have to be placed in parallel. As an example, increasing  $N$  to 10 required 10 preamplifiers, and 60 passive SC delay stages (10 stages for the 10 dipole channels multiplied by 6 parallel structures to achieve the sample rate as outlined in Section II). It is anticipated that duplicating the SC stages increases the area proportionally, but does not significantly add to the power consumption. Since the power budget of the system is dominated by the low-noise preamplifiers, parallelization appears a viable proposition for further investigation [10].

The system can be extended to allow recording from additional electrodes by adding further preamplifiers and sampling capacitors. The additional preamplifiers then operate in a master-slave arrangement sharing a single CM stage and reducing the power overhead per channel due to the CM feedback stage [8]. In the current implementation all preamplifiers are continuously powered ON to provide a stable, non-switched interface to the tissue. Whether it would be possible to reduce the bias current in the input stage during the amplification phase (or whenever  $\phi_{1a}/\phi_{1c}$  are low) to save power without affecting the interface quality is also a subject for future investigation.

Also note that the ADC sample rate in the proposed system is determined by the input signal characteristics (to satisfy the Nyquist criterion), and that this is lower than the rate required in a fully digital implementation where the input signals must be sampled in intervals of  $\Delta T$ . Keeping the ADC conversion speed low compared to a digital design (about 1:20 in a final system) yields further potential advantages in power consumption and reduced converter complexity.

A digital implementation of the delay-and-add backend (excluding ADC) would consume about 30 mW per channel. This estimate is based upon digital design simulation by the Xilinx ISE toolset, and a signal activity estimate of 0.25 combined with power consumption data for the austriamicrosystems 0.8  $\mu\text{m}$  library [9]. It reduces to about 7 mW in an estimate using 0.35  $\mu\text{m}$  library parameters and



compares with the  $<2$  mW measured for the current proposed analogue systems. However, the digital implementation benefits over-proportionally from technology scaling, thus potentially reducing the power advantage of the analogue approach in advanced CMOS technologies. The area of the analogue S&H circuit is favourable with  $<0.2$  mm<sup>2</sup> compared to about 1.7 mm<sup>2</sup> in the digital circuit. Both approaches yield possible size reduction at smaller technology nodes.

In terms of absolute input-referred noise density, voltage gain, dynamic range and gain matching the proposed circuits meet the target for advanced neural recording (see [24], [24] and Table I for benchmarking parameters). Testing the expanded system with more tripoles using natural nerve traffic remains the subject of ongoing research. Overall, the measured data obtained from the 2-channel systems confirm that systems of this type have significant advantages compared to the earlier continuous-time systems.

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**Robert Rieger** was born in Duesseldorf, Germany. He received the intermediate diploma in electrical engineering and the B.Eng. degree (1st hon.) in Electrical and Electronics Engineering from Chemnitz University of Technology, Germany, and the University of Kent, U.K., in 1998 and 2000 respectively. He earned the Ph.D. degree in electronic and electrical engineering from University College London (UCL), U.K. in 2004.

During 2001-2004 he has been a Research Assistant at UCL and later at the University of Bath, U.K. He then joined the Industry & Medical business unit of austriamicrosystems AG, Rapperswil, Switzerland, where he was concerned with the design of low-power integrated circuits. He joined the Electrical Engineering Department at National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2006, where he is now an Associate Professor.

Dr. Rieger is the founding officer of the IEEE Engineering in Medicine and Biology Society (EMBS) Tainan Chapter and a member of the IEEE Technical Committees on *BioCAS*, *VLSI Systems and Applications* (VTA) and *CAS Education & Outreach* (CASEO) of the CAS Society. He is also an Associate Editor for *IEEE Transactions on Biomedical Circuits & Systems*. His research interests are in the area of low-power electronics for biomedical application and bio-chip design.



**John Taylor** was born at Wanstead, Essex, UK, in 1952. He received the BSc and PhD degrees from Imperial College, London University, London, UK, in 1973 and 1984, respectively.

During 1984-1985, he held the post of Research Fellow in the Department of Electrical Engineering, University of Edinburgh, Scotland, where worked on certain theoretical aspects of switched-capacitor filter design.

He joined the Department of Electronic and Electrical Engineering at University College London in 1985 and subsequently, in 2002, the Department of Electronic and Electrical Engineering at the University of Bath, Bath, UK, where he holds the position of Professor of Microelectronics and Optoelectronics and Director of the University *Centre for Advanced Sensor Technologies*. His research interests are in the fields of analogue and mixed analogue and digital system design, including communication systems and low-power implantable systems for biomedical and rehabilitation applications.

Professor Taylor has published more than 140 technical papers in international journals and conferences and has co-edited a handbook on filter design.